6. (Amended) The method of Claim 5 wherein said d) further comprises:

placing a spacer in said data structure of said plurality of logical names in responsive to a determination that there was no configuration bit at said address in said configuration block.

8. (Amended) A computer implemented method of generating an order of loading data into a programmable logic device comprising the steps of:

a) accessing a data structure comprising a plurality of logical names corresponding to a plurality of addresses;

b) accessing a data structure specifying an order in which said plurality of addresses are to be loaded into said programmable logic device;

c) ordering said plurality of logical names from step a) based on the order specified in said data structure in step b); and

d) storing said ordered plurality of logical names from step c) in a data structure within computer readable memory, wherein said ordered plurality of logical names describe an order of loading data into a programmable logic device.

17. (Amended) The method of Claim 14 wherein said d) comprises:

determining whether there is a configuration bit at an address of said plurality of addresses in a configuration block.

18. (Amended) The method of Claim 17 wherein said d) further comprises:

placing a spacer in said data structure of said plurality of logical names responsive to a determination that there was no configuration bit at said address in said configuration block.